

MSLIN-98-004



July 14, 2000

2815
#5/6 Election
Group
7/24/00

To: Commissioner of Patents and Trademarks

Washington, D.C. 20231

Attn: Art Unit 2815 - L. Cruz

From: George O. Saile, Reg. No. 19,572

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Subject: | Serial No.: 09/258,911 03/01/99 |

M.S. Lin

HIGH PERFORMANCE SUB-SYSTEM DESIGN
AND ASSEMBLY

| _ Art Group: 2815 L. Cruz _ |

RESPONSE TO RESTRICTION REQUIREMENT

This is in response to the Restriction or Election
Requirement in the Office Action dated 07/05/00. In that
Office Action, restriction was required to one of two stated

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on July 13, 2000.

George O. Saile, Reg.# 19572

Signature/Date

George O. Saile 7/13/00

Inventions under 35 U.S.C. 121. The Inventions stated are Group I - Claims 1-25 to a semiconductor device, classified in Class 257, subclass 777 and Group II - Claims 26-37 to a process, classified in Class 438, subclass 1+.

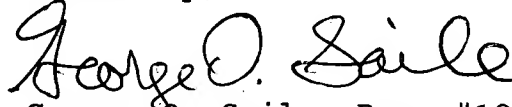
Applicant provisionally elects to be examined the Invention described by the Examiner as Group II - Claims 26-37 drawn to a process classified in Class 438, subclass 1+. This election is made with traverse of the requirement under 37 C.F.R.1.143 for the reasons given in the following paragraphs.

The Examiner is respectfully requested to reconsider the Requirement for Restriction given in the Office Action. The Examiner gives the reason for the distinctness of the two inventions as (1) that the process as claimed can be used to make other and materially different products or (2) that the product as claimed can be made by another and materially different process (MPEP 806.05(f)). However, upon reading the product Claims against the process Claims one can readily see that the product Claims are directed to "a multiple inter-connected integrated circuit chip structure comprising a first integrated circuit chip and a second integrated circuit chip" and the process Claims are directed to "a method of forming a multiple integrated circuit chip structure", it is necessary to obtain claims in both the product and method claim language. The method Claims necessarily use the product and vice versa. The field of search must necessarily cover both the method

class/subclass 438/1+ and products class 257/777 in addition to other related Classes and subclasses to provide a complete and adequate search. The fields of search for the Group I and Group II inventions are clearly and necessarily co-extensive. The Examiner's suggestion that "the product as claimed can be made by another and materially different process. In the instant case unpatentability of Group I invention does not necessarily imply unpatentability of Group II invention since the device of Group I invention could be made without necessarily simultaneously but instead at different times forming internal circuits on a first and second semiconductor wafers", is very speculative and really has nothing to do with the Claims as presented in this Patent Application. Further, it is respectfully suggested that these reasons are insufficient to place the additional cost of a second Patent Application upon the Applicants. Therefore, it is respectfully requested that the Examiner withdraw this restriction requirement for these reasons.

Withdrawal of the Restriction Requirement and the Allowance of the present Patent Application is requested.

Sincerely,

A handwritten signature in cursive script that reads "George O. Saile". The signature is written in dark ink and is positioned above the printed name.

George O. Saile, Reg. #19572